Design And Implementation Of DADDA Tree Multiplier Using Adiabatic Logic On FPGA

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Abstract – Low power circuit designs have been an important issue VLSI design areas. Multipliers play a major role in high performance systems. The Dadda tree multiplier is considered as faster than a simple array multiplier and is an efficient implementation of a digital circuit which is multiplies two integers such multiplier which is effective both in terms of speed and power. Adiabatic logic style is said to be an attractive solution for low power electronic applications. By using Adiabatic techniques energy dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. In this work ECRL(Efficient Charge Recovery Logic) based Dadda tree multiplier is compared with Wallace tree multiplier. xilinx 9.1 tools are used for simulation and to implement Spartan 3E family FPGA KIT.

Index Terms – Dadda tree multiplier,Adiabatic logic,ECRL.

1. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications .In high performance systems such as microprocessor, DSP etc addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operation dominates the execution time. That's why, there is need of high speed multiplier. The demand of high speed processing has been increasing as a result of expanding computer and signal processing applications.

1.1 DIFFERENT MULTIPLIERS

An efficient multiplier should have following characteristics:-

Accuracy

Speed

Area

Power

Multiplication process has three main steps:

- Partial product generation.
- Partial product reduction.
- Final addition.

For the multiplication of an n-bit multiplicand with an m bit multiplier, m partial products are generated and product formed is n + m bits long. Here we discuss about four different types of multipliers which are

- Booth multiplier.
- Combinational multiplier.
- Wallace tree multiplier.
- Dadda tree multiplier.
- Array multiplier.
- Sequential multiplier.

A. Dadda Tree Mulitiplier

The Dadda multiplier is a hardware multiplier design invented by computer scientist Luigi Dadda in 1965. It is similar to the Wallace multiplier, but it is slightly faster (for all operand sizes) and requires fewer gates (for all but the smallest operand sizes).[1]

In fact, Dadda and Wallace multipliers have the same 3 steps:

1. Multiply (logical AND) each bit of one of the arguments, by each bit of the other, yielding n^2 results. Depending on position of the multiplied bits, the wires carry different weights, for example wire of bit carrying result of $a_2 b_3$ is 32.
2. Reduce the number of partial products to two by layers of full and half adders.
3. Group the wires in two numbers, and add them with a conventional adder.

However, unlike Wallace multipliers that reduce as much as possible on each layer, Dadda multipliers do as few reductions as possible. Because of this, Dadda multipliers have a less

expensive reduction phase, but the numbers may be a few bits longer, thus requiring slightly bigger adders.

To achieve this, the structure of the second step is governed by slightly more complex rules than in the Wallace tree. As in the Wallace tree, a new layer is added if any weight is carried by three or more wires. The reduction rules for the Dadda tree, however, are as follows:

- Take any three wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each three input wires.
- If there are two wires of the same weight left, and the current number of output wires with that weight is equal to 2 (modulo 3), input them into a half adder. Otherwise, pass them through to the next layer.
- If there is just one wire left, connect it to the next layer.

This step does only as many adds as necessary, so that the number of output weights stays close to a multiple of 3, which is the ideal number of weights when using full adders as 3:2 compressors.

However, when a layer carries at most three input wires for any weight, that layer will be the last one. In this case, the Dadda tree will use half adder more aggressively (but still not as much as in a Wallace multiplier), to ensure that there are only two outputs for any weight. Then, the second rule above changes as follows:

- If there are two wires of the same weight left, and the current number of output wires with that weight is equal to 1 or 2 (modulo 3), input them into a half adder. Otherwise, pass them through to the next layer

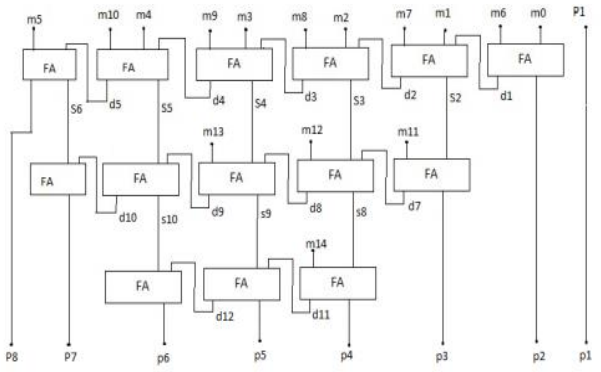

Fig. 1 4x4 Dadda tree mulitiplier

2. ADIABATIC LOGIC

Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits get smaller and faster, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation.

A. ADIABATIC CIRCUIT

Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy.

Unlike traditional CMOS circuits, which dissipate energy during switching, adiabatic circuits reduce dissipation by following two key rules:

- Never turn on a transistor when there is a voltage potential between the source and drain.
- Never turn off a transistor when current is flowing through it.

While this is an area of active research, current techniques rely heavily on transmission gates and trapezoidal clocks to achieve these goals.

B. CMOS ADIABATIC CIRCUITS

There are some classical approaches to reduce the dynamic power such as reducing supply voltage, decreasing physical capacitance and reducing switching activity. These techniques are not fit enough to meet today's power requirement. However, most research has focused on building adiabatic logic, which is a promising design for low power applications.

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation. Each phase of the power clock gives user to achieve the two major design rules for the adiabatic circuit design.

C. 2N2N-2P FUNCTION BLOCK

The design of high-speed and low-power VLSI architectures needs efficient processing units, which are optimized for the speed and power consumption. Hence, the trend has been to search for techniques to reduce the power dissipation, low power operation, and designing for energy recovery and recycling. Energy recovery is proving to be a promising approach for the design of low power VLSI circuits. The primary advantage of these circuits results from its inherent characteristics of deriving a constant current from the power clock get the FETs working with the minimum voltage between the source and drain terminals. The basic complementary function Block of 2N-2N2P.

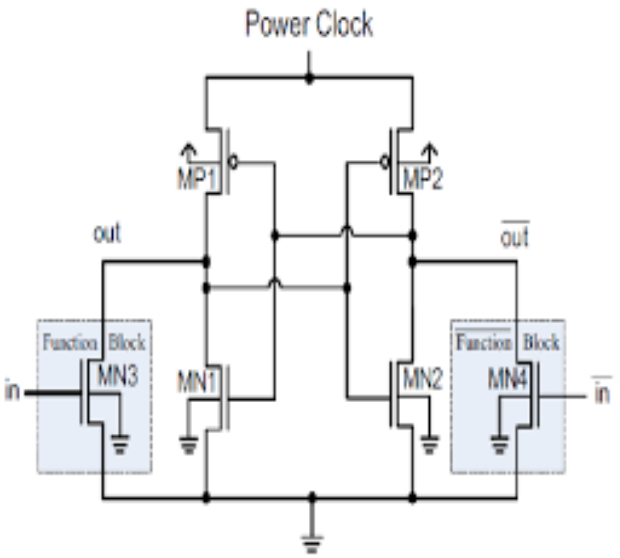

Fig.2 FUNCTION BLOCK 2N2N-2P

D. 2N2N-2P LOGIC

The name 2N-2N2P is based on the convention of using the number of transistors in the inverter gate. Figure 1 illustrates the CMOS circuit of 2N-2N2P XNOR/XOR logic. Since there are energy losses due to nonzero voltage drop needed to turn on unidirectional devices, 2N-2N2P is covered under partial Energy Recovery Logic (ERL) family. 2N-2N2P has cross-coupled inverters to latch the output. 2N-2N2P is a revised version of Efficient Charge Recovery Logic (ECRL). Similar to ECRL, the pull-down network, which is helpful in fast discharging during the evaluation phase, is complementary to each other.

E. 2N2N-2P WALLACE TREE MULTIPLIER

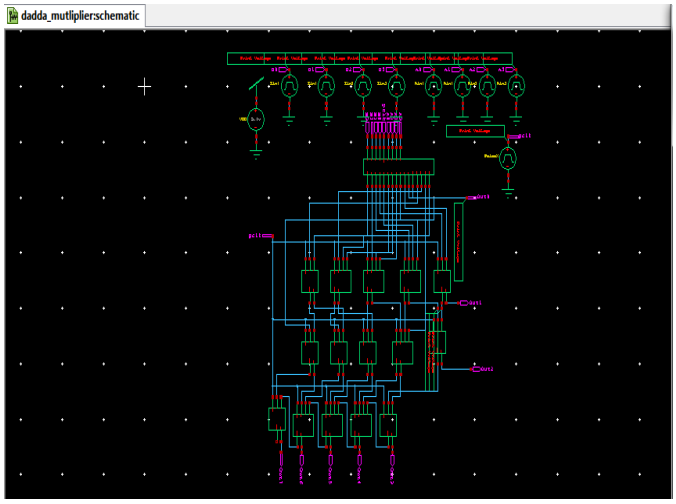

Fig.3 2n2n-2p Dadda tree multiplier

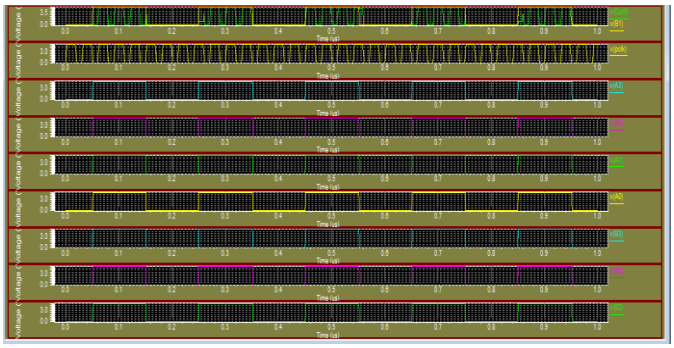

Fig.4 2n2n-2p Wallace tree multiplier output waveform

```
* BEGIN NON-GRAPHICAL DATA

Power Results
VVDD from time 0 to 1e-006
Average power consumed -> 9.242019e-002 watts
Max power 4.208307e-001 at time 5.15063e-007
Min power 5.178791e-007 at time 0


* END NON-GRAPHICAL DATA
*

* Parsing                        0.01 seconds
* Setup                          0.09 seconds
* DC operating point             0.46 seconds
* Transient Analysis            13.27 seconds
* Overhead                       1.61 seconds
* ----------------------------------------
* Total                         15.43 seconds

* Simulation completed

* End of T-Spice output file
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Fig 5 2n2n-2p Dadda tree multiplier power result

3. SPARTAN 3E FPGA OUTPUT RESULT

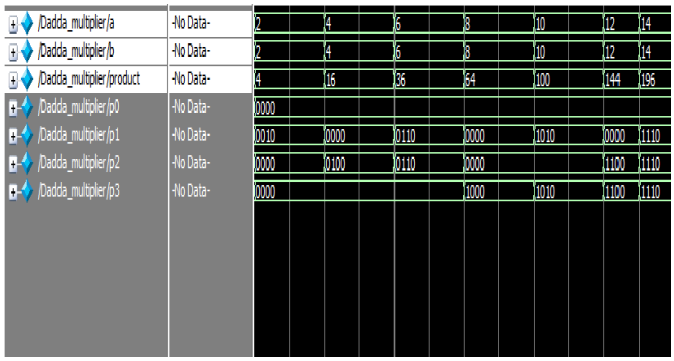

Fig. 6. Dadda tree multiplier waveform result

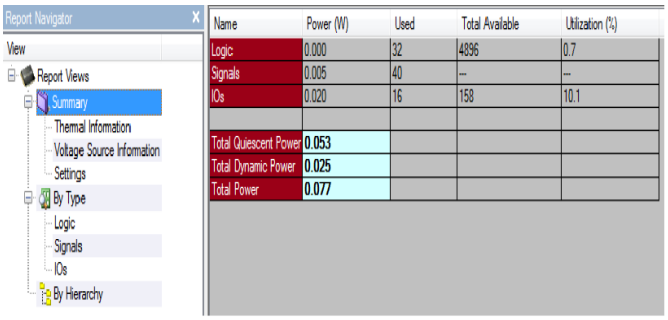

Fig 7. Dadda tree multiplier power result

4. COMPARISON TABLE of Tanner EDA Tool

TANNER EDA TOOL	POWER
Wallace tree multiplier	1.056561e-001
Dadda tree multiplier	9.242019e-002

5. COMPARISON TABLE OF SPARTAN 3E FPGA OUTPUT

FPGA SPARTAN 3E	POWER
Wallace tree multiplier	80mw
Dadda tree multiplier	77mw

6. CONCLUSIONS

It is concluded from above that energy consumption at lower frequencies is minimum in case of ECRL followed by CMOS, 2N2N2P i.e. leakage losses are minimum in ECRL. As the frequency of operation increases energy consumption starts decreasing. It is minimum and it is most efficient adiabatic logic technique followed by 2N2N2P and ECRL. At above process remains no longer adiabatic as a result energy consumption of all three adiabatic techniques becomes greater than CMOS. Frequency of operation of adiabatic logic could be increased to few hundred of MHz if load capacitance is reduced. Area consumption of adiabatic logic is greater than standard CMOS which its main disadvantage. Thus the applications are limited, for example a pace maker where energy saving is main target.

For the future work, 2N-2P ECRL LOGIC will be implemented in *WALLACE TREE MULTIPLIER* AND *DADDA TREE MULTIPLIER* can improve speed,power consumption etc.

REFERENCES

[1] C.S. Wallace, "A Suggestion for a Fast Multiplier," IEEE Trans. Electronic Computers, vol. 13, no. 1, pp. 14-17, Feb. 1964.
[2] L.Dadda, "Some schemes for parallel multipliers,"Alta Frequenza, vol.34
[3] Naveen K Gahlan, Prabhat, Jasbir Kaur " Implementation of Wallace Tree Multiplier Using Compressor" International Journal of Computer & Technology
[4] Implementation of Dadda and Array Multiplier Architectures Using Tanner Tool
[5] Design and Analysis of CMOS Based DADDA Multiplier. IJCEM,VOL .16 ISSUE 6, NOV 2013
[6] A Design Technique for Faster Dadda Multiplier
[7] A new hybrid multiplieusing Dadda and Wallace method. IEEE Vol issue 13-14 Feb. 2014
[8] An efficient floating-point multiplier design using combined booth and dadda algorithms. 30th June 2014. Vol. 64 No.3